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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 PENNSYLVANIA AVE. N.W.
WASHINGTON,, DC 200373202

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on December 6, 2005. Claim 4 of the application was amended. Claims 1-4 of the application are pending. This office action is made final.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al.** (U.S. Patent 5,274,568) in view of **Hasegawa** (U.S. Patent 6,041,168) and further in view of **Hasegawa** (U.S. Patent 5,528,511).

4.1 **Blinne et al.** teaches method of estimating logic cell delay time. Specifically, as per Claim 1, **Blinne et al.** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach that for at least one circuit of the plurality of circuits, the library further comprises logical operation information. **Hasegawa** '168 teaches that for at least one circuit of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Blinne et al.** with the system of **Hasegawa** '168 that included for at least one circuit of the plurality of circuits, the library further comprising logical operation information, because delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one

circuit; and the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. **Hasegawa** '511 teaches the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Blinne et al.** and **Hasegawa** '168 with the system of **Hasegawa** '511 that included the logical operation information representing correspondence between logical state

transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for each signal path of the at least one circuit being based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process (Col 2, Lines 61-65).

Blinne et al. and **Hasegawa** '168 do not expressly teach that when making a delay analysis of each signal path of the logic circuit that comprises the at least one circuit, a delay time is selected from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches how when making a delay analysis of each signal path of the logic circuit that comprises the at least one circuit, a delay time is selected from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition

triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

4.2 As per Claim 2, **Blinne et al.** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach that for each of the plurality of circuits, the library further comprises logical operation information. **Hasegawa** '168 teaches that for each of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach the logical operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal for each circuit of the plurality of circuits, and the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. **Hasegawa** '511 teaches the logical operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal for each circuit of the plurality of circuits, and the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation

information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Blinne et al. and **Hasegawa** '168 do not expressly teach that when making a delay analysis of each signal path through the plurality of circuits, a delay time of each path between a plurality of input terminals and a selected output terminal of the at least one circuit is selected from the delay time information, wherein if the selected output terminal transitions from a low state to a high state the delay time is selected based on the input terminal of the plurality of input terminals whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if the selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal of the plurality of input terminals whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches how when making a delay analysis of each signal path through the

plurality of circuits, a delay time of each path between a plurality of input terminals and a selected output terminal of the at least one circuit is selected from the delay time information, wherein if the selected output terminal transitions from a low state to a high state the delay time is selected based on the input terminal of the plurality of input terminals whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if the selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal of the plurality of input terminals whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

4.3 As per Claim 3, **Blinne et al.** teaches a method for making a delay analysis of a logic circuit (Col 1, Lines 7-13); comprising the steps of:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information, and delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach the delay analysis library comprising logic operation information. **Hasegawa** '168 teaches library comprising logic operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach the logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal for at least one circuit of the plurality of circuits; and the

delay information for each path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. **Hasegawa** '511 teaches the logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal for at least one circuit of the plurality of circuits; and the delay information for each path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Blinne et al. and **Hasegawa** '168 do not expressly teach if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high

state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

4.4 As per Claim 4, **Blinne et al.** teaches a computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer perform a process for executing a delay analysis method for a logic circuit, the computer readable medium causing a computer to execute the method (Col 2, Lines 42-50); wherein the method comprises:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information and delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach the delay analysis library comprising logic operation information. **Hasegawa** '168 teaches that the library comprising logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of each one of the plurality of circuits; and the delay information for each path of the at least one circuit of the plurality of circuits is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit. **Hasegawa** '511 teaches logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of each one of the plurality of circuits; and the delay information for each path of the at least one circuit of the plurality of circuits is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at

least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Blinne et al. and **Hasegawa** '168 do not expressly teach if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

Blinne et al. and **Hasegawa** '168 do not expressly teach performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit.

Hasegawa '511 teaches performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit (Col 3, Lines 5-26).

Response to Amendments

5. Applicants' amendments, filed on December 6, 2005 have been considered. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive.

5.1 As per the applicants' argument that "With respect to claim 1, the combination of Blinne et al., Hasegawa `168 and Hasegawa `511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the logical state transitions at the input and output terminals of a logical circuit, where the analysis library stores delay time information based on correspondence between the input terminal logical state transitions and the output terminal logical state transitions, and the delay information is selected based upon certain input/output terminal signal transitions; the combination of Blinne et al., Hasegawa `168 and Hasegawa `511 does not use input terminal logical state transitions, output terminal logical state transitions and delay information in the same manner as the present invention; Blinne et al. do not teach or suggest **determining delay time based on the current logical state of a circuit** and how the input signal transitions will affect that logical state; Blinne et al. ignore the logic operation of the analyzed logic circuit by independently recording each of the many inputs of the logic circuit; inputs not being measured are fixed to a predetermined logic level while measuring the delay time of the remaining input; in calculating the maximum delay time for the logic

circuit, Blinne et al. uses the delay time of the input with the longest delay time; ... Hasegawa `168 does not even teach or suggest signal transitions, but instead adds a series of maximum delay times together to determine a propagation delay; Hasegawa `511 still rely upon maximum delay times, stored in the arcs between nodes, for propagation delay time calculations; Hasegawa `511 does not teach or suggest determining delay time for "each signal path of said at least one circuit" based on the logical state transitions at the input and output terminals; Hasegawa `511 also specifies that **certain signal paths are "invalid"** due to their rise/fall characteristics for certain signal paths, and that no signal path that contains an "invalid" identifier is used for delay calculations; ... the combining of Blinne et al., Hasegawa `168 and Hasegawa `511 with each other does not remove this fundamental deficiency which permeates each of the references; in the three references, the propagation delay time for a logic circuit is arrived at **using maximum delay times**, and there is no discussion of using the input signal transitions and the current logical state of the logic circuit as index to a propagation delay time that is representative of how the logic circuit actually operates; the delay analysis in Hasegawa `511 is for a single-input, single-output circuit; the analysis disclosed for Figure 1 discards certain propagation paths, while claim 1 specifically recites that the propagation analysis is made for "each signal path of said at least one circuit"; Hasegawa `511 specifies that certain signal paths are "invalid" due to their rise/fall characteristics for certain signals, and that no signal path that contains an "invalid" identifier is used for delay calculations; there is no teaching or suggestion in the combination of references that indicates that "invalid" signal paths are used in calculating delay time for logical state transitions; Hasegawa `511 cannot teach or suggest "making a delay analysis of each signal path of said at least one circuit" as recited in claim 1, since Hasegawa `511 clearly and

unequivocally rejects making a delay analysis of those signal paths that are deemed to be "invalid" and not necessary for inclusion", the examiner respectfully disagrees.

Blinne et al. teaches the delay analysis system having a delay analysis library (Col 1, Lines 9-13); and comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Hasegawa '168 teaches that for at least one circuit of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35).

Hasegawa '511 teaches the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in

the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65).

Hasegawa '511 teaches how when making a delay analysis of each signal path of the logic circuit that comprises the at least one circuit, a delay time is selected from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65).

As per the argument that Blinne et al. do not teach or suggest **determining delay time based on the current logical state of a circuit,** the Examiner takes the position that the applicant's method does not determine delay time based on the current logical state of a circuit.

As per the applicant's argument that "Hasegawa `511 also specifies that **certain signal paths are "invalid"** due to their rise/fall characteristics", the Examiner takes the position that whether one specifies certain paths as invalid or not does not affect the method, since the path that does not contribute to the output signal transition is ignored both in Hasegawa `511 and the applicant's method.

As per the argument that the propagation delay time for a logic circuit is arrived at **using maximum delay times,** the Examiner takes the position that this is not true as shown by Figs. 2-5 of Hasegawa `511 and the method of marking some paths as invalid.

5.2 As per the applicants' argument that "while Applicant admits that Hasegawa `511 does show determining delay time on the basis of an input signal's effect on a circuit's logical state, Hasegawa `511 does it in a completely different manner than the present invention; Hasegawa `511 discloses, an invalidness specification means that specifies arcs (i.e., signal paths) that have invalid data and arcs where either the rise or fall (but not both) of a signal is valid; therefore, if a signal path has been declared to be invalid, or valid only for one of rise or fall time, then Hasegawa `511 does not teach or suggest the recitations of claim 1 that recite that delay information is available for each signal path of the at least one circuit, and that input signal transitions for causing both low-to-high and high-to-low output terminal state transitions are to be considered; in contrast, the present invention recited in claim 1 uses delay time information for all signal paths of a particular circuit; the Patent Office is failing to appreciate the distinction between Hasegawa `511, which avoids evaluating invalid signal paths, and evaluation of all signal paths, as recited in claim 1; the fact that the present invention recited in claim 1 does not

ultimately use timing information from certain signal paths should not be confused with the declaration of a signal path being invalid, as disclosed in Hasegawa `511", the examiner takes the position that Hasegawa `511considers each signal path as shown in Fig. 2 to Fig. 5; additionally, whether one specifies certain paths as invalid or not does not affect the method, since the path that does not contribute to the output signal transition is ignored both in Hasegawa `511 and the applicant's method, as explained in Paragraph 5.1 above.

5.3 As per the applicants' argument that "the combination of Blinne et al., Hasegawa `168 and Hasegawa `511 fails to teach or suggest that a delay time is selected from delay time information according to input terminal and output terminal logical state transitions, as recited in claim 1; the Patent Office alleges that Hasegawa `511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne et al.; Hasegawa `511 does not teach or suggest determining delay time based on **the current logical state of a circuit** and the logical state transitions at the input and output terminals; Hasegawa `511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations; Hasegawa `511 does not use all the types of logical state transitions present between the input and output terminals of all paths in a logic circuit when selecting a delay time for a particular signal propagation path through the logic circuit; Applicant submits that the Patent Office cannot fulfill the "all limitations" prong of a prima facie case of obviousness with respect to claim 1, as required by In re Vaeck", the examiner respectfully disagrees as explained in paragraph 7.1 above.

Hasegawa '511 teaches the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

As per the argument that Blinne et al. do not teach or suggest **determining delay time based on the current logical state of a circuit,** the Examiner takes the position that the applicant's method does not determine delay time based on the current logical state of a circuit.

As per the argument that Hasegawa `511 uses the maximum delay time between two nodes in performing its delay calculations, the Examiner takes the position that this is not true as shown by Figs. 2-5 of Hasegawa `511 and the method of marking some paths as invalid.

5.4 As per the applicants' argument that "one of skill in the art would not be motivated to combine the three references; none of the references teaches or suggests providing delay information for a circuit that is based upon the type of signal transitions present at the circuit's input and output terminals as represented by stored logical operation information; Blinne et al., Hasegawa `168 and Hasegawa `511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis; in addition, none of the references teaches or suggests that a delay time is selected from delay time information for each circuit path according to the type of logical state transitions

present at both the input and output terminals of a circuit, as recited in claim 1; since none of the references teaches or suggests these features of claim 1, Applicant submits that one of ordinary skill in the art would not have been motivated to combine the three references; thus, Applicant submits that the Patent Office cannot fulfill the motivation prong of a prima facie case of obviousness with respect to claim 1, as required by In re Dembiczak and In re Zurko", the examiner takes the position that the references provide the necessary motivations as described below.

Blinne et al. teaches the delay analysis system having a delay analysis library (Col 1, Lines 9-13); and comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Hasegawa '168 teaches that for at least one circuit of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35).

Hasegawa '511 teaches the logical operation information representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; and the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by the logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42;

Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65).

As per the argument that Blinne et al., Hasegawa `168 and Hasegawa `511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis, the Examiner takes the position that this is not true as shown by Figs. 2-5 of Hasegawa `511 and the method of marking some paths as invalid.

Conclusion

ACTION IS FINAL

6. Applicant's arguments with respect to claim rejections under 35 USC § 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
December 31, 2005

Paul L. Rodriguez 1/5/06
Primary Examiner
Art Unit 2125